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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,387	02/02/2001	Stanley N. Protigal	2898.2US (88-070.7)	2208
24247	7590	05/17/2004		
EXAMINER				SEFER, AHMED N
ART UNIT				PAPER NUMBER
				2826

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/776,387

Applicant(s)

PROTIGAL ET AL.

Examiner

A. Sefer

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address -- *AN*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 04 March 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 3-5 and 8-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 3-5 and 8-10 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachments(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____

5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

Response to Amendment

1. The amendment filed on March 4, 2004 has been entered; no new claims have been added.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (e) the invention was described in–
 - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
 - (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii (“Fujii”)

USPN 4,654,689.

Fujii discloses (see figs. 5 and 6, col. 4, lines 60-68 and abstract) a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising a regulator circuit 21 for receiving an electrical power signal; a semiconductor substrate 10; active circuit devices 20 formed the semiconductor substrate; and an on-chip capacitor (fig. 6B) having at least a portion thereof formed in active area of the semiconductor substrate or an on-chip capacitor C comprising a planar type capacitor (as in claim 4) having at least a portion thereof formed in active area of the semiconductor substrate, the on-chip capacitor being operably

coupled in a shunt configuration to the regulator circuit and operably coupled in a shunt configuration to the active circuit devices.

As for claims 5, Fujii discloses a first node and a second node, one node of the first and second nodes comprising a poly layer 24 and the other node of the first and second nodes comprising a channel 51.

4. Claims 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii.

Fujii discloses (see figs. 5 and 6, col. 4, lines 60-68 and abstract) a semiconductor device for connection to a carrier substrate configured to provide power and ground thereto, the semiconductor device comprising a semiconductor substrate 10 having active circuit elements 20 formed on an active area thereof; at least one regulator circuit 21 for receiving power; and at least one capacitor (fig. 6B) on the semiconductor substrate comprising a planar type capacitor (as in claim 9), at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor being operably coupled shunt configuration to the at least one regulator circuit and to the active circuit elements.

As for claims 10, Fujii discloses a first node and a second node, one node of the first and second nodes comprising a poly layer 24 and the other node of the first and second nodes comprising a channel 51.

5. Claims 3 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Kazerounian et al. ("Kazerounian") USPN 5,014,097.

Kazerounian discloses in figs. 2-8 a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising a regulator circuit 108 for receiving an electrical power signal; a semiconductor substrate 257/422; active circuit devices 101/400

formed the semiconductor substrate; and an on-chip capacitor 110 having at least a portion thereof formed in active area of the semiconductor substrate or an on-chip capacitor C comprising a planar type capacitor (as in claim 4) having at least a portion thereof formed in active area of the semiconductor substrate, the on-chip capacitor being operably coupled in a shunt configuration to the regulator circuit and operably coupled in a shunt configuration to the active circuit devices.

6. Claims 8 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kazerounian.

Kazerounian discloses in figs. 2-8 a semiconductor device for connection to carrier substrate configured to provide power and ground thereto, the semiconductor device comprising a semiconductor substrate 257/422 having active circuit elements 101/422 formed on an active area thereof; at least one regulator circuit 108 for receiving power; and at least one capacitor 110 on the semiconductor substrate comprising a planar type capacitor (as in claim 9), at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor being operably coupled shunt configuration to the at least one regulator circuit and to the active circuit elements.

As for providing filtering capacitance for the semiconductor device recited in the claims 3 and 8, a recitation of an intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazerounian in view of Patel et al. ("Patel") USPN 4,737,830.

Kazerounian discloses the device structure as recited in the claim, but does not specifically disclose a first and second nodes comprising a poly and a channel respectively.

Patel discloses in figs. 3B and 9-12 a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising; a semiconductor substrate 28; active circuit devices formed the semiconductor substrate; and an on-chip capacitor 16 having at least a portion thereof formed in active area of the semiconductor substrate or an on-chip capacitor C comprising a planar type capacitor (as in claim 4); and a first node and a second node, one node of the first and second nodes comprising a poly layer 18 and the other node of the first and second nodes comprising a channel 24.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Patel's teachings with Kazerounian's device since that reduce voltage spikes as taught by Patel.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shearer et al. USPN 4,871,979 discloses (see fig. 6 and col. 8, 3-20) a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising and active circuit devices formed the semiconductor substrate; and an on-chip capacitor providing filtering capacitance.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

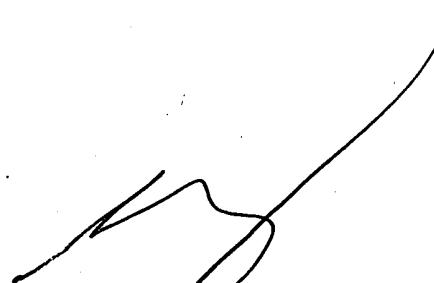
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
May 11, 2004



NATHAN J. FLYNN
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